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EXAMINER
DHARIA, PRABODH M

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 07/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/742,383	LEE, MOO JIN	
	Examiner	Art Unit	
	Prabodh M Dharia	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. **Status:** Receipt is acknowledged of papers submitted on 06-13-2003 under amendments have been placed of record in the file. Claims 1-26, are pending in this action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3,6,8-10,15-19,22,23,25,26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katakura et al. (5,754,154) in view of Kikuo et al. (5,250,937).

Regarding Claim 1, Katakura et al. teaches a charge characteristic compensating circuit (106, figure 8, Col. 9, Lines 33-36, Col. 5, Lines 33-43, Lines 52,53) for a liquid crystal display panel (101, figure 8, Col. 9, Lines 20,21) including a plurality of liquid crystal cells arranged at each intersection between data lines and gate lines (Scan Line) (figure 6, Col. 6, Lines 20-25) to control a light transmissivity in response to data signals from the data lines, (Col. 9, Line 57 to Col. 10, Line 4) and a plurality of switching devices for switching the data signals to be applied from the data lines to the liquid crystal cells (Col. 9, Lines 36-41) in response to signals on the gate lines (Scan Lines), the circuit comprising (Col. 6, Lines 8-10): a voltage supply for generating a gate voltage required for the gate lines (Scan Lines) (figure 3, Col. 5, Lines 25-29); a gate line driver for applying the gate voltage from the voltage supply to the gate lines to drive the gate lines (figure 3, Col. 5, Lines 25-29, Col. 9, lines 45-54); and a current controller for responding to a change in the ambient temperature to change an amount of current (Col. 5, Lines

31-43, Col. 9, lines 20-65) of the gate voltage to be applied from the voltage supply to the gate line driver (Col. 5, Lines 27-30, Col. 9, Lines 45-65).

However, Katakura fails to teach Scan Lines, which are connected to the Gate Lines to drive LCD display and a resistor and a thermistor for responding to change in ambient temperature.

However, it is well known to one in the ordinary skill in the art that in an active matrix type LCD the scan lines are connected to the gate lines and video information is connected to drain of the pixel driving transistor. The reference cited of Kikuo et al. also teaches gate lines and gate line driver are connected to scan line and scan line driver respectively (Col. 20, Lines 23-25, Col. 22, Lines 26,27, Col. 18, Lines 44-49) and it is also well known to one in the ordinary skill in the art as the change in ambient temperature changes impedance of the resistor and thermistor, which in turn changes current flowing through them as well as panel capacitor. This in turn changes voltage drop across resistor and thermistor and also change charge across display panel (Col. 13, Lines 19-68).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Kikuo et al. teaching in Katakura et al. teaching to have a high luminance output, accurate gray levels, minimizes display artifacts and flickering.

Regarding Claim 2, Katakura et al. teaches the current controller (Col. 9, Lines 20-44) and correction circuit is connected between the voltage supply and the gate line driver (Col. 5, Lines 27-40). Kikuo et al. teaches said resistor and said thermistor are connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also

the gate line driver by using the corrected voltage super imposed on the clock CL1 that generates horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 3, Katakura et al. teaches the current controller (Col. 9, Lines 20-44) and correction circuit is connected between the voltage supply and the gate line driver (Col. 5, Lines 27-40). Kikuo et al. teaches said resistor and said thermistor are connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also the gate line driver by using the corrected voltage super imposed on the clock CL1 that generates horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 6, Katakura et al. teaches a charge characteristic compensating circuit (106, figure 8, Col. 9, Lines 33-36, Col. 5, Lines 33-43, Lines 52,53) for a liquid crystal display panel (101, figure 8, Col. 9, Lines 20,21) including a plurality of liquid crystal cells arranged at each intersection between data lines and gate lines (Scan Line) (figure 6, Col. 6, Lines 20-25, Col. 9, Lines 31-54)) to control a light transmissivity in response to data signals from the data lines, (Col. 9, Line 57 to Col. 10, Line 4) and a plurality of switching devices for switching the data signals to be applied from the data lines to the liquid crystal cells (Col. 9, Lines 36-41) in response to signals on the gate lines (Scan Lines), the circuit comprising (Col. 6, Lines 8-10): a voltage supply for generating a gate voltage required for the gate lines (Scan Lines) (figure 3, Col. 5, Lines 25-29); a gate line driver for applying the gate voltage from the voltage supply to

the gate lines to drive the gate lines (figure 3, Col. 5, Lines 25-29); and a current controller for responding to a change in the ambient temperature to change an amount of current (Col. 5, Lines 31-40) of the gate voltage to be applied from the voltage supply to the gate line driver (Col. 5, Lines 27-30).

However, Katakura fails to teach Scan Lines, which are connected to the Gate Lines to drive LCD display and a resistor and a thermistor for responding to change in ambient temperature.

However, it is well known to one in the ordinary skill in the art that in an active matrix type LCD the scan lines are connected to the gate lines and video information is connected to drain of the pixel driving transistor. The reference cited of Kikuo et al. also teaches gate lines and gate line driver are connected to scan line and scan line driver respectively (Col. 20, Lines 23-25, Col. 22, Lines 26,27, Col. 18, Lines 44-49) and it is also well known to one in the ordinary skill in the art as the change in ambient temperature changes impedance of the resistor and thermistor, which in turn changes current flowing through them as well as panel capacitor. This in turn changes voltage drop across resistor and thermistor and also change charge across display panel (Col. 13, Lines 19-68).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Kikuo et al. teaching in Katakura et al. teaching to have a high luminance output, accurate gray levels, minimizes display artifacts and flickering.

Regarding Claim 8, Kikuo et al. teaches the thermistor is a negative temperature coefficient thermistor (Col. 13, Lines 56-61).

Regarding Claim 9, Katakura et al. teaches a charge characteristic compensating circuit (106, figure 8, Col. 9, Lines 33-36, Col. 5, Lines 33-43, Lines 52,53) for a liquid crystal display panel (101, figure 8, Col. 9, Lines 20,21); a voltage supply for generating a gate voltage required for the gate lines (Scan Lines) (figure 3, Col. 5, Lines 25-29, Col. 9, Lines 45-54); a gate line driver for applying the gate voltage from the voltage supply to the gate lines to drive the gate lines (figure 3, Col. 5, Lines 25-29, Col. 9, Lines 20-65); and a current controller for responding to a change in the ambient temperature to change an amount of current (Col. 5, Lines 31-40, Col. 9, Lines 31-44) of the gate voltage to be applied from the voltage supply to the gate line driver (Col. 5, Lines 27-30, Col. 9, Lines 45-65). Kikuo et al. also teaches gate lines and gate line driver are connected to scan line and scan line driver respectively (Col. 20, Lines 23-25, Col. 22, Lines 26,27, Col. 18, Lines 44-49); a voltage converter generating a high level gate voltage (Col. 15, Lines 55-60); a gate line controller including a resistor and a thermistor (Col. 13 Lines 42-50), receiving the high level gate voltage from the voltage converter (Col. 17, Lines 23-26) and supplying a controlling signal that varies as an ambient temperature varies (Col. 8, Lines 8-11, Col. 29, Lines 43-62); and a gate line driver receiving the controlling signal from the gate line controller and driving a gate line (Col. 29, Lines 43-64, Col. 32, Lines 9-20).

Regarding Claim 10, Katakura et al. teaches the gate line (Scan Line) controller is a current controller such that the controlling signal received by the gate line (Scan Line) driver includes an electrical current, an amount of which varies as the ambient temperature varies (Col. 5, Lines 31-40).

Regarding Claim 15, Kikuo et al. teaches gate line controller is a voltage divider such that the controlling Signal received by the gate line driver includes a voltage, a level of which varies as the ambient temperature varies (Col. 16, Lines 39-47, Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 16, Kikuo et al. teaches the thermistor is a negative temperature coefficient thermistor (Col. 13, Lines 56-61); the voltage divider decreases the voltage as the ambient temperature increases (Col. 29, Lines 42-62).

Regarding Claim 17, Kikuo et al. teaches the voltage divider (Col. 13, Lines 37-68) includes a thermistor (Col. 17, Lines 28-30, Col. 29, Lines 50-60).

Regarding Claim 18, Kikuo et al. teaches the thermistor is a negative temperature coefficient thermistor (Col. 13, Lines 56-61).

Regarding Claim 19, Kikuo et al. teaches the voltage divider (Col. 13, Lines 61-65) further includes said resistor (Col. 13, Lines 61-65) such that the resistor is connect-between the voltage converter (Col. 13, Lines 37,38) and an input to said gate line driver (Col. 16, Lines 39-47, Col. 29, Lines 42-62, Col. 32, Lines 9-20) and the negative temperature coefficient thermistor (Col. 13, Lines 56-58) is connected between ground (reference voltage) (figure27,

Col. 29, Lines 42-55) and the input to the gate line driver (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 22, Katakura et al. teaches a charge characteristic compensating circuit (106, figure 8, Col. 9, Lines 33-36, Col. 5, Lines 33-43, Lines 52,53) for a liquid crystal display panel (101, figure 8, Col. 9, Lines 20,21); comprising: a voltage supply for generating a gate voltage required for the gate lines (Scan Lines) (figure 3, Col. 5, Lines 25-29, Col. 9, Lines 20-65); a gate line driver for applying the gate voltage from the voltage supply to the gate lines to drive the gate lines (figure 3, Col. 5, Lines 25-29, Col. 9, Lines 20-65); and a current controller for responding to a change in the ambient temperature to change an amount of current (Col. 5, Lines 31-40, Col. 9, Lines 31-54) of the gate voltage to be applied from the voltage supply to the gate line driver (Col. 5, Lines 27-30, Col. 9, Lines 45-54).

Kikuo et al. teaches a gate line driver for applying the gate voltage from the voltage supply to the gate lines to drive the gate lines (figure 7b, Col. 10, Lines 1-16,); and a current controller for responding to a change in the ambient temperature to change an amount of current of the gate voltage (Col. 11, Line 65 to Col. 12, Line 5, Col. 13, Lines 37-65, Col. 17, Lines 17-39) to be applied from the voltage supply to the gate line driver and supplying a controlling signal that varies by way of a resistor (Col. 16, Lines 39-63, Col. 29, Lines 42-62, Col. 32, Lines 9-20) and thermistor as an ambient temperature varies; and driving a gate line according to said controlling signal (Col. 11, Line 65 to Col. 12, Line 5, Col. 13, Lines 37-65, Col. 14, Lines 48-68, Col. 17, Lines 17-39)

Regarding Claim 23, Katakura et al. teaches the gate line (Scan Line) controller is a current controller such that the controlling signal received by the gate line (Scan Line) driver includes an electrical current, an amount of which varies as the ambient temperature varies (Col. 5, Lines 31-40).

Regarding Claim 25, Katakura et al. teaches the gate lines (Scan Lines), the circuit comprising (Col. 6, Lines 8-10): a voltage supply for generating a gate voltage required for the gate lines (Scan Lines) (figure 3, Col. 5, Lines 25-29); a gate line driver for applying the gate voltage from the voltage supply to the gate lines to drive the gate lines (figure 3, Col. 5, Lines 25-29); and a current controller for responding to a change in the ambient temperature to change an amount of current (Col. 5, Lines 31-40) of the gate voltage to be applied from the voltage supply to the gate line driver (Col. 5, Lines 27-30).

Regarding Claim 26, Kikuo et al. teaches the thermistor is a negative temperature coefficient thermistor (Col. 13, Lines 56-61); the voltage divider decreases the voltage as the ambient temperature increases (Col. 29, Lines 42-62).

4. Claims 4,5,7,11-14,24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katakura et al. (5,754,154) in view of Kikuo et al. (5,250,937) as applied to claims 1-3,6,8-10, 15-19,22,23,25,26 above, and further in view of Marks et al. (5,119,215).

Regarding Claim 4, Katakura et al. teaches the current controller (Col. 9, Lines 20-44) and correction circuit is connected between the voltage supply and the gate line driver (Col. 5, Lines 27-40). Kikuo et al. teaches a resistor and a thermistor connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also the gate line driver by using the corrected voltage super imposed on the clock CL1 that generates horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

However, Katakura et al. modified by Kikuo fails to teach the thermistor is a positive temperature coefficient thermistor.

However, Marks et al. teaches the thermistor is a positive temperature coefficient thermistor (Col. 4, Lines 49-52).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Marks et al. teaching in Katakura et al. modified by Kikuo et al. teaching to have a high luminance output, and minimizes display artifacts.

Regarding Claim 5, Marks et al. teaches the thermistor is a positive temperature coefficient thermistor (Col. 4, Lines 49-52).

Regarding Claim 7, Katakura et al. teaches the current controller (Col. 9, Lines 20-44) and correction circuit is connected between the voltage supply and the gate line driver (Col. 5, Lines 27-40). Kikuo et al. teaches said resistor and said thermistor connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also the gate line driver by using the corrected voltage super imposed on the clock CL1 that generates

horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 11, Marks et al. teaches the thermistor is a positive temperature coefficient thermistor (Col. 4, Lines 49-52). It is well known to one in the ordinary skill in the art that the positive temperature coefficient thermistor increases impedence with the increase in temperature and with the voltage applied the current controller decreases the amount of current as the ambient temperature increases.

Regarding Claim 12, Kikuo et al. teaches the current controller includes a thermistor (Col. 17, Lines 28-30, Col. 29, Lines 50-60).

Regarding Claim 13, Marks et al. teaches the thermistor is a positive temperature coefficient thermistor (Col. 4, Lines 49-52).

Regarding Claim 14, Kikuo et al. teaches the current controller (Col. 17, Lines 28-30, Col. 29, Lines 50-60), further includes said resistor and said thermistor connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also the gate line driver by using the corrected voltage super imposed on the clock CL1 that generates horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 24, Marks et al. teaches the thermistor is a positive temperature coefficient thermistor (Col. 4, Lines 49-52). It is well known to one in the ordinary skill in the art that the positive temperature coefficient thermistor increases impedence with the increase in temperature and with the voltage applied the current controller decreases the amount of current as the ambient temperature increases.

5. Claims 20, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katakura et al. (5,754,154) in view of Kikuo et al. (5,250,937) as applied to claims 1-3,6-10,12,14,15-19,22,23,25,26 above, and further in view of Noma et al. (6,184,631 B1).

Regarding Claim 20, Katakura et al. teaches the current controller (Col. 9, Lines 20-44) and correction circuit is connected between the voltage supply and the gate line driver (Col. 5, Lines 27-40). Kikuo et al. teaches a resistor and a thermistor connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also the gate line driver by using the corrected voltage super imposed on the clock CL1 that generates horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

However, Katakura et al. modified by Kikuo fails to teach the voltage divider further includes a positive temperature coefficient thermistor such that the positive temperature coefficient thermistor is connected between the voltage converter and an input to the gate line driver.

However, Noma et al. teaches the voltage divider further includes a positive temperature coefficient thermistor such that the positive temperature coefficient thermistor is connected between the voltage converter and an input to the gate line driver (Col. 12, Lines 65-67, Col. 10,

Lines 58-60) and Kikuo et al. teaches the negative temperature coefficient thermistor (Col. 13, Lines 56-58) is connected between ground (reference voltage) (figure27, Col. 29, Lines 42-55) and the input to the gate line driver (Col. 29, Lines 42-62, Col. 32, Lines 9-20) .

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Noma et al. teaching in Katakura et al. modified by Kikuo et al. teaching to have a high luminance output, accurate gray levels, minimizes display artifacts and flickering by supplying constant liquid current to LCD display.

Regarding Claim 21, Noma et al. teaches teaches the voltage divider includes a positive temperature coefficient thermistor such that the positive temperature coefficient thermistor is connected between the voltage converter and an input to the gate line driver and a resistor such that the resistor is connected between ground and the input to the gate line driver (Col. 12, Line 62 to Col. 13 Line 6, Col. 10, Lines 58-60)

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is informed that all of the other additional cited references render the claims obvious.

Response to Arguments

7. Applicant's arguments filed 06-13-2003 have been fully considered but they are not persuasive.

Applicant argues the cited reference of Katakura et al. fails to teach compensating of charge characteristic of the panel and changing the amount of current of the gate voltage to be applied to the gate line based on an ambient temperature.

Examiner disagrees, as charge of the panel is represented by letter "Q". It is well known to one in the ordinary skill in the art, that Q=di/dt, where "i" represents current and "t" represents the time interval. The cited reference of Katakura et al. teaches compensating of charge characteristic of the panel (Col. 5, Lines 33-43, Lines 52,53) and changing the amount of current of the gate voltage to be applied to the gate line based on an ambient temperature. (It is well known to one in the ordinary skill in the art that in an active matrix type LCD the scan lines are connected to the gate lines and video information is connected to drain of the pixel driving transistor, and the temperature affects the impedance not only of the gate but also of the drain and source, which affects the current flow through and the voltage of the switch controlling pixel of the LCD panel); (Col. 9, Lines 20-30, Lines 45-58, Col. 5, Lines 31-43).

Applicant argues, cited references do not teach a current controlling devices that includes a resistor and thermistor.

Examiner disagrees, as Kiluo et al teaches a current controlling devices that includes a resistor and thermistor (Col. 17, Lines 27-39, Col. 13, Lines 37-68, Col. 14, Lines 48-65).

8. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge

generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Katakura et al. teaches a display panel is driven by applying drive signals thereto while compensated charge characteristic circuit correcting the drive signals based on the detected current signal variation because of change in ambient temperature. As a result the display panel achieves better transmissivity (brightness) and better gradation display. Kikuo et al. teaches controlling of transmissivity (brightness) using resistor, thermistor and switches controlling current flowing through the resistor network. Combination does teach applicant's invention and they do obviate.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 703-605-1231. The examiner can normally be reached on M-F 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-3054938. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9341 for regular communications and 703-872-9341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

PD

Au2673

July 11, 2003

Amare Mengistu
Primary Examiner